REMARKS

Claims 1-15 remain in the application. Claims 1-15 stand rejected. No claims have been amended.

In the final rejection, the Examiner withdrew the previous rejection in light of the previous response. However, the Examiner entered a new ground of rejection of all of the claims.

The Examiner rejected claims 1-15 under 35 U.S.C. § 103 as unpatentable over Vergnes et al. in view of Perrott.

Each of the independent claims of this application is directed to a clock recovery circuit. Each of the independent claims requires a series connection of "an error filter, a gain element and a frequency accumulator."

The purpose of the claimed gain element in that series connection is set forth on page 7 of the specification, lines 4-12. There, the Applicants state:

> The output of the phase detector/comparator 50, which represents the error between the recovered clock and the received data signal, is coupled through a loop filter 60 and gain stage 70 for application to a frequency accumulator 80. The gain is set so that the accumulator 80 overflows when the difference frequency f_d between the received data clock f_R and frequency f_N is a prescribed value.

Thus, the gain stage provides for adjustable control of overflow/underflow.

Neither of the references alone or in combination suggests the claimed invention.

Figure 1 of Vergnes et al. is directed to a frequency synthesizer. Figures 6 and 7 of Vergnes et al. refer to phase lock loops using the synthesizer of Figure 1 in two different embodiments (Figure 6 and Figure 7). The Examiner has relied upon the embodiment of Figure 6 for the rejection.

All embodiments shown in Vergnes et al. have an output frequency that is determined by digital words. Turning to column 6, lines 53-60 state:

> The phase signal is generated on the transmitter side by means of a phase generator (a modulo counter). This counter is periodically transmitted in a bitstream time clock and this value, a digital tuning word, represents the digital value of the phase. On the receiver side, this digital value must be recovered and filtered, in order to cope with channel disturbances. The recovered, compared and filtered signal will drive a frequency synthesizer.

From Vergnes et al.'s description of the Figure 6 embodiment, there is no need for a gain stage. Specifically, the specification teaches away from modifications suggested by the Examiner. The insertion of a gain stage in the Figure 6 embodiment of Vergnes et al., would have no function and thus the specification teaches away from modifications suggested by the Examiner.

The Perrott reference is directed to a bit error rate detector. In a discussion of the prior art in Figure 1, Perrott does show a phase lock loop and does suggest a "loop amplifier." However, there is no series connection of an error filter, a gain element and a frequency accumulator. Perrott does not show a gain-accumulator combination.

With respect to the rational for the combination of references, the Examiner states, on page 4 of the Office Action:

> Vergnes et al. and Perrot [*sic.*] teachings teach in the same field of endeavor. Because loop amplifier and filter are implemented in the conventional PLL, one of ordinary skill in the art at the time the invention was made would have been motivated to modify Vergnes et al. PLL to further include a loop amplifier.

The Examiner's conclusion is incorrect. As noted above, Vergnes et al. has no need for a loop amplifier and therefore it would not be obvious to add one. The only motivation that exists for adding a loop amplifier to Vergnes et al. would be to meet the terms of the claim in a classical hindsight approach. The Examiner has demonstrated no reason for modifying Vergnes et al. by adding a loop amplifier. The Examiner has failed to establish a *prima facie* case of obviousness by establishing a rational for the combination of references.

As noted above, the purpose of the gain element in the specification is to provide adjustable control of overflow or underflow.

For the reasons indicated, Applicants respectfully request reconsideration of the Examiner's new rejection and allowance of the application.

Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 01-0484 and please credit any excess fees to

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such deposit account.

Respectfully submitted,

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